What is claimed is:

1. A micromirror device comprising:

a DRAM memory cell with a polysilicon-to-substrate storage capacitor; (fig 3)

a mirror superstructure electrically connected to said memory cell; and (Col 7, li 29-33)

reset electrodes positioned by said mirror superstructure. (col 4, li 35-36)

2. The micromirror device of Claim 1, wherein said DRAM memory cell further comprises: 314

a single CMOS transistor having an inherent junction capacitor and electrically connected to said polysilicon-to-substrate storage capacitor;

a bit-line providing data to said memory cell;

a word address line; and

a mirror address node connected to an output of said memory cell.

3. The micromirror device of Claim 2, wherein said polysilicon-to-substrate capacitor encircles said mirror address node.

4. The micromirror device of Claim 2, wherein the area of said polysilicon-to-substrate capacitor takes up the majority of an area of said mirror superstructure.

5. The micromirror device of Claim 2, wherein a majority of a stored charge is stored on said polysilicon-to-substrate capacitor.

6. The micromirror device of Claim 2, wherein said polysilicon-to-substrate capacitor electrically is in parallel with said inherent junction capacitor.

7. The micromirror device of Claim 2, wherein an implant is applied to provide a flat band voltage operating range from 0 to +5 volts for said polysilicon-to-substrate capacitor.

8. The micromirror device of Claim 2, wherein a signal to the bit address line is inverted.

9. The micromirror device of Claim 2, wherein said mirror address node is located at a center of said memory cell.

10. The micromirror device of Claim 2 further comprising an array of said memory/mirror cells.

11. The micromirror device of claim 2 further comprising additional light shielding over said mirror address node.

12. The micromirror device of Claim 1 further comprising:

an oxide layer;

a hinge and yoke layer above said metal layer;

a mirror metal layer above said hinge and yoke layer; and

wherein said reset electrodes are formed on said oxide layer;

13. The micromirror device of Claim 12 wherein said metal layer extends over said address node.

14. The micromirror device of Claim 12, wherein said "reset" and "reset bar" electrodes are horizontally connected across said array to enable phase reset mode of operation.

15. The micromirror device of Claim 12, wherein said cell address node is connected to said mirror beam by means of a hinge post, said hinge, said yoke, and a mirror post.

16. The micromirror device of Claim 12, wherein said mirror over failed CMOS cell, always turns OFF.

17. The micromirror device of Claim 12, wherein:

said "reset" and "reset bar" electrode steady state values are set at +20 and -15 volts, respectively;

said "reset" and "reset bar" electrodes are switched to -15V and +20 volts, respectively, to reset the micromirror mirrors;

said "reset" and "reset bar" electrodes are switched to +5 volts and 0 volts, respectively, to set said micromirror mirrors to their new state;

the mirror beam is addressed at 0 volts to rotate said micromirror mirror -10° OFF; and

said mirror beam is addressed at +5 volts to rotate said micromirror mirror +10° ON.

18. A micromirror display comprising:

a light source providing a beam of light on a light path;

a color filter on said light path for filtering said beam of light;

condensing optics on said light path;

a one transistor one capacitor micromirror with polysilicon-to-substrate storage capacitor on said light path for selectively modulating said beam of light; and

a projection lens for focusing said selectively modulated beam on light on an image plane.

19. The micromirror display of Claim 19, wherein said color filter is a rotating color wheel.

20. The micromirror display of Claim 19, wherein said color filter is a color splitting and combining prism.